CLAIMS:

1. A circuit arrangement for an AC voltage supply of a plasma display panel, the arrangement comprising at least a transistor bridge (T1, T2, T3, T4), an input voltage (U0), a capacitor (Cp) of the plasma cell and a charging current circuit, the charging current circuit being supplied with an auxiliary charging current (u1), characterized in that the DC voltage converter is connected in parallel to the auxiliary charging voltage (u1).

2. A circuit arrangement as claimed in claim 1, characterized in that the DC voltage converter is a boost converter.

3. A circuit arrangement as claimed in claim 1 or 2, characterized in that the boost converter comprises a transistor (TA), a diode (DA) and an inductor (LA).

4. A circuit arrangement as claimed in any one of the preceding claims, characterized in that the three connections of a boost converter are connected to the positive side of the capacitor (Csb), to ground and to the positive side of the capacitor (Csa).

5. A circuit arrangement as claimed in any one of claims 1 to 4, characterized in that the auxiliary charging voltage (u1) has a value exceeding half the value of the input voltage (U0).

6. A circuit arrangement as claimed in any one of claims 1 to 5, characterized in that the charging current circuit comprises at least a series combination of an auxiliary transistor (T11), a first diode (D1) and a first coil (L1).

7. A circuit arrangement as claimed in any one of claims 1 to 6, characterized in that the auxiliary charging voltage (u1) is applied to an auxiliary capacitor (Csa).

8. A circuit arrangement as claimed in any one of claims 1 to 7, characterized in that the capacitance (Csa) of the auxiliary capacitor is much larger than the capacitor (Cp) of the plasma cell.

9. A circuit arrangement as claimed in any one of the preceding claims, characterized in that the auxiliary charging voltage (u1) is generated from an auxiliary discharging voltage (u2) by a DC converter.

10. A circuit arrangement as claimed in claim 3, characterized in that the transistor (TA) via its source has a first connection point shared with the capacitance (Csa) of the auxiliary voltage and with the ground terminal of the input voltage (U0) and via its drain has a connection point shared with the coil (LA) and the anode of the diode (DA).

11. A circuit arrangement as claimed in claim 3 or 10, characterized in that the diode (DA) with its cathode has a connection point shared with the transistor (T11) of the charging oscillator circuit and the positive side of the capacitor (Csa).

12. A circuit arrangement as claimed in any one of claims 3, 10 or 11, characterized in that the coil (LA) with its other end is connected at least to the transistor (T12) of a discharging oscillator circuit.

13. A circuit arrangement as claimed in any one of the preceding claims, characterized in that the value of the auxiliary charging voltage (u1) is more than 50% of the value of the input voltage (U0).

14. A circuit arrangement for the AC voltage supply of a plasma display panel, the arrangement comprising at least a transistor bridge (T1, T2, T3, T4), an input voltage (U0), a capacitor (Cp) of the plasma cell and a discharging circuit, the discharging circuit supplying an auxiliary discharging voltage (u2), characterized in that in addition a DC voltage converter is connected in parallel to the auxiliary discharging voltage (u2).

15. A circuit arrangement as claimed in claim 14, characterized in that the DC voltage converter is a buck converter.

16. A circuit arrangement as claimed in claim 14 or 15, characterized in that the buck converter comprises a transistor (TB), a diode (DB) and an inductor (LB).

17. A circuit arrangement as claimed in any one of the claims 14 to 16, characterized in that the three connections of a buck converter are connected to the positive side of the input voltage (U0), to ground and to the positive side of the capacitor (Csb).

18. A circuit arrangement as claimed in any one of the claims 14 to 17, characterized in that the auxiliary discharging voltage (u2) has a value that falls short of half the value of the input voltage (U0).

19. A circuit arrangement as claimed in any one of the claims 14 to 18, characterized in that the discharging circuit comprises at least a series combination of an auxiliary transistor (T12), a second diode (D2) and a second coil (L2).

20. A circuit arrangement as claimed in any one of the claims 14 to 19, characterized in that the auxiliary discharging voltage (u2) is applied to an auxiliary discharging capacitor (Csb).

21. A circuit arrangement as claimed in any one of the claims 14 to 20, characterized in that the capacitance (Csb) of the auxiliary discharging capacitor by far exceeds the capacitance (Cp) of the plasma cell.

22. A circuit arrangement as claimed in any one of the claims 14 to 21, characterized in that the auxiliary discharging voltage (u2) is generated from the discharge of the capacitor (Cp) and stabilized by a DC voltage converter.

23. A circuit arrangement as claimed in claim 22, characterized in that the DC voltage converter compensates for the losses caused by the commutation and takes the necessary power from the input voltage (Uo).

24. A circuit arrangement as claimed in claim 16, characterized in that the transistor (TB) via its drain has a first common connection point with the positive side of the

input voltage (U0) and via its source has a common connection point with the coil (LB) and the anode of the diode (DB).

25. A circuit arrangement as claimed in claim 16 or 23, characterized in that the coil (LA) is connected to the transistor (T12) of the discharging circuit.

26. A circuit arrangement as claimed in any one of the claims 16, 23 or 25, characterized in that with its other end the coil (LA) is connected at least to the transistor (T11) of a charging circuit.

27. A circuit arrangement as claimed in any one of the claims 14 to 26, characterized in that the value of the auxiliary discharging voltage (u2) is less than 50% of the value of the input voltage (U0).

28. A circuit arrangement as claimed in any one of the claims 1 to 27, characterized in that the auxiliary voltages (u1) and (u2) and the associated DC voltage converters are used for a plurality of independent bridge circuits which utilize a common input voltage (Uo).

29. A plasma display panel comprising a circuit arrangement for supplying AC voltage to the plasma display panel, which circuit arrangement comprises at least a transistor bridge (T1, T2, T3, T4), an input voltage (U0), a capacitor (Cp) of the plasma cell and a charging circuit, the charging circuit being supplied with an auxiliary charging voltage (u1), characterized in that the DC voltage converter is connected in parallel to the auxiliary charging voltage (u1).